PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Manufacturer Test Mode Pin
DATE:	March 29, 2019
AFFECTED DOCUMENT:	PCI Express Card Electromechanical Specification Revision 4.0, Version 0.9
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Part I

1. Summary of the Functional Changes

High Volume Manufacturing (HVM) and other manufacturer test processes benefit from the ability to set Add-in Card (AIC) modes that enable multiplexing of standard connector pins for test specific use. This ECR defines a method to allow the system to enable a Manufacturer Test Mode (MFG) on the AIC Module through the standard interface connector prior to shipping the module.

This MFG Mode ECR is consistent with that already approved in the PCI-SIG SFF Connector Workgroup, SFF Manufacturing Mode ECR for 60 Day Member Review.

2. Benefits as a Result of the Changes

Support for a MFG state, set by the system using standard interface signals, allows AIC MFG modes and signal multiplexing to support test signaling without requiring a separate connector. Separate connectors add cost, not only added connector costs, but also for non-interface connector insertion handling. Manual cabling is unreliable, and prevents effective use of automation (i.e. robotoic insertion/removal).

Setting a MFG state and the associated pin signal multiplexing through the standard connector reduces manufacturing and AIC design cost and enables automation.

3. Assessment of the Impact

The MFG pin state is an optional feature, only implemented if AIC manufacturers require it, and associated functionality is disabled prior to the AIC being shipped. It is desired that this MFG pin be assigned as close to the mechanical key connector area as possible. The RSVD pins available closest to the mechanical key are in the x4 key area, pins A-19 and A-32. This ECR proposes A19 be specified as MFG.

4. Analysis of the Hardware Implications

Repurposes reserved pin A-19 to be the MFG Test pin.

5. Analysis of the Software Implications

No impact to operating system or device driver software.

6. Analysis of the C&I MFG Implications

Does not impact solution interoperability, therefore no C&I impact.

7. Analysis of the Virtualization Implications

Does not impact virtualization software or hardware, therefore no virtualization impact.

Part II

Detailed Description of the change

Change Section 2. Auxiliary Signals, page 21 add MFG signal description:

- MFG (optional): A manufacturer test mode signal. Pin functionality is defined by the Add-in Card (AIC) manufacturer and must be disabled in non-manufacturing environments.

Add a new sub-section 2.7 to Section 2. Auxiliary Signals, page 34 as follows:

2.7. MFG Signal (Optional)

The MFG signal is an optional signal applicable only to Add-in Cards (AIC) that support a manufacturer-specific test mode, and as such all functional requirements are outside the scope of this specification. On System Boards, MFG pin is not connected.

Electrical specifications of the MFG signal is defined in Table 1.

MFG pin must be terminated as specified in section 9.2.6 Auxiliary Signal Conductor AC Match Termination, and must not have any impact to AIC operation.

Change Section 2.7 to 2.8, and add MFG to DC Specification section, page 35 as follows:

2.8. Auxiliary Signal Parametric Specifications

2.8.1. DC Specifications

Table 1 lists the auxiliary signal DC sSpecifications for PERST#, WAKE#, CLKREQ#, SMBus, PWRBRK#, and MFG.

Table 1: Auxiliary Signal DC Specifications – PERST#, WAKE#, CLKREQ#, SMBus, PWRBRK#, and MFG

Change Section 6.1, Table 37, add MFG pin to connector Pinout table, page 86 as follows:

6.1. Connector Pinout

Table 37 shows the pinout definition for the x1, x4, x8, and x16 PCI Express connectors. The auxiliary pins are identified in the shaded areas.

Table 37: PCI Express Connectors Pinout

Pin #	Side B		Side A	
	Name	Description	Name	Description
1	+12V	+12 V power	PRSNT1#	Hot-Plug presence detect
2	+12V	+12 V power	+12V	+12 V power
3	+12V	+12 V power	+12V	+12 V power
4	GND	Ground	GND	Ground
5	SMBCLK	SMBus (System Management Bus) clock	JTAG2	TCK (Test Clock), clock input for JTAG interface
6	SMBDAT	SMBus (System Management Bus) data	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	+3.3 V power	JTAG5	TMS (Test Mode Select)
9	JTAG1	TRST# (Test Reset) resets the JTAG interface	+3.3V	+3.3 V power
10	+3.3Vaux	+3.3 V auxiliary power	+3.3V	+3.3 V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental reset
Mechanical Key				
12	CLKREQ#	Clock Request Signal	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK-	
15	PETn0	Transmitter differential pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
End of the x1 Connector				
19	PETp1	Transmitter differential pair, Lane 1	MFG	Manufacturer Test Mode
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground

Change Section 9.2.6. Auxiliary Signal Conductor AC Match Termination, page 152, change pin A19 from RSVD to MFG:

- A x4 Add-in Card or connector requires four additional auxiliary signals be terminated:
  – A19 MFG

Change Section 9.3.1. Sentry Ground Vias Adjacent to Auxiliary Signal Vias, page 154, change pin A19 from RSVD to MFG:

A x4 connector requires four more auxiliary signals be isolated:
MFG (pin A19)